

AMENDMENTS

Claims

The following is a copy of Applicant's claims:

1. (Original) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins;
compressing the first plurality of data units using a first compression technique; and
compressing the second plurality of data units using a second compression technique.
2. (Original) The method of claim 1, further comprising, prior to the steps of compressing:
determining a timing complexity for the first plurality of data units; and
determining a timing complexity for the second plurality of data units.
3. (Original) The method of claim 1, wherein the first plurality of data units corresponds to clock signals and the second plurality of data units corresponds to non-clock signals.
4. (Original) The method of claim 1, wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.
5. (Original) The method of claim 1, wherein the first plurality of data units have a different timing complexity than the second plurality of data units.
6. (Original) The method of claim 1, wherein the first plurality of data units have a different vector data volume than the second plurality of data units.

7. (Original) The method of claim 1, wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.
8. (Original) The method of claim 1, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins.
9. (Original) The method of claim 1, further comprising the step of:
formatting the first plurality of data units independently from the second plurality of data units.
10. (Original) The method of claim 1, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.
11. (Original) The method of claim 1, wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.
12. (Original) A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins;
determining that the first plurality of data units have a first compressibility characteristic;
and
determining that the second plurality of data units have a second compressibility characteristic.

13. (Original) The method of claim 12, further comprising the step of:
compressing the first plurality of data units independently from the second plurality of data units.

14. (Original) The method of claim 12, wherein the first plurality of DUT pins are
clock-pins and the second plurality of DUT pins are non-clock-pins.

15. (Original) The method of claim 12, wherein the test data file is one of a STIL
(standard test interface language) file and a WGL (waveform generation language) file.

16. (Original) The method of claim 12, wherein the first plurality of data units have a
different timing complexity, a different vector data volume, and more repetitive data patterns than
the second plurality of data units.

17. (Original) A system for adaptively compressing test data to be provided to a device
under test (DUT), the system comprising:

memory configured to store a test data file that includes a first plurality of data units
corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to
a second plurality of DUT pins; and

a processor operative to:

compress the first plurality of data units using a first compression technique; and
compress the second plurality of data units using a second compression technique.

18. (Original) The system of claim 17, wherein the processor is operative to:
determine a timing complexity for the first plurality of data units; and
determine a timing complexity for the second plurality of data units.

19. (Original) The system of claim 17, wherein the first plurality of data units
correspond to clock signals and the second plurality of data units correspond to non-clock signals.

20. (Original) The system of claim 17, wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.

21. (Original) The system of claim 17, wherein the first plurality of data units have a different timing complexity than the second plurality of data units.

22. (Original) The system of claim 17, wherein the first plurality of data units have a different vector data volume than the second plurality of data units.

23. (Original) The system of claim 17, wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.

24. (Original) The system of claim 17, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins.

25. (Original) The system of claim 17, further comprising the step of:
formatting the first plurality of data units independently from the second plurality of data units.

26. (Original) The system of claim 17, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

27. (Original) The system of claim 17, wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables the second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

28. (Original) A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:

memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins; and

a processor that is operative to:

determine that the first plurality of data units have a first compressibility characteristic;

determine that the second plurality of data units have a second compressibility characteristic.

29. (Original) The system of claim 28, wherein the processor is operative to:
compress the first plurality of data units independently from the second plurality of data units.

30. (Original) The system of claim 28, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins.

31. (Original) The system of claim 28, wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

32. (Original) The system of claim 28, wherein the first plurality of data units have a different timing complexity, a different vector data volume, and more repetitive data patterns than the second plurality of data unit